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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,474	12/12/2003	Ali H. Burney	174/286	9607

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,474	BURNEY, ALI H.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Rangasayee (US 6,404,225 B1).

Regarding claim 1, Rangasayee discloses at least in Figs. 3, 4, and 6, a programmable logic resource (200) comprising:

an input/output (I/O) buffer (160, 162, 164, 166; col. 5, lines 15+) that receives data from circuitry external (see bidirectional I/O 170-173) to the programmable logic resource and generates a plurality of outputs (170-173);

a crossbar switch (250, 252, and 280) that receives the plurality of outputs from the I/O buffer and generates a plurality of outputs (col. 5, lines 1+), wherein the crossbar switch is configured to send at least one of the plurality of outputs from the I/O buffer to a corresponding one of the plurality of outputs of the crossbar switch (Fig. 4; col. 6, lines 58+);

an intellectual property block (102, 104) that receives the plurality of outputs of the crossbar switch for processing (col. 6, lines 12+).

Regarding claim 2, Rangasayee discloses at least in Figs. 3, 4, and 6, that the programmable logic resource of I/O buffer:

receives the data at I/O ports (170-173) located along the periphery of the programmable logic resource; and

decodes (col. 5, lines 49+) the data to generate the plurality of outputs.

Regarding claim 3, Rangasayee discloses a package (IC; col. 1, lines 31+) in which the programmable logic resource is mounted.

Regarding claim 4, Rangasayee discloses at least in Figs. 3, 4, and 6, that the package has pins (inherently coupled to 170-173) through which the circuitry external to the programmable logic resource sends data, wherein the data is further routed from the pins to the I/O buffer (col. 5, lines 49+).

Regarding claims 5-14, as for the recitation, "digital processing system", "processing circuitry", "memory", "printed circuit board", and/or their interconnections, as set forth in the claims, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987). Also, the recitation discussed above are implied in col. 9, lines 7+.

Regarding claim 9, Rangasayee discloses at least in Figs. 3, 4, and 6, a package (IC; col. 1, lines 31+) having a plurality of pins (inherently coupled to 170-173), the package having embedded therein a programmable logic resource (200) having a plurality of input/output (I/O) ports (170-173) located along the periphery of the programmable logic resource and coupled to the plurality of pins, wherein the programmable logic resource comprises circuitry (250, 252, 280) configured to send data from at least one of the plurality of I/O ports (170-173) to a corresponding one of a plurality of data ports in an intellectual property block (102, 104) for processing.

Regarding claim 10, Rangasayee discloses at least in Figs. 3, 4, and 6, that at least one of the plurality of pins (that is connected to 170-173) is coupled to a nearest available one of the plurality of I/O ports (170-173).

Regarding claim 11, Rangasayee discloses at least in Figs. 3, 4, and 6, that the programmable logic resource further comprises an I/O buffer (160, 162, 164, 166; col. 5, lines 15+) that receives the data from the plurality of I/O ports and decodes (col. 5, lines 49+) the data for output to the circuitry.

Regarding claim 12, Rangasayee discloses at least in Figs. 3, 4, and 6, that circuitry is a configurable crossbar switch (250, 252, 280; col. 6, lines 58+).

Regarding claim 13, Rangasayee discloses at least in Figs. 3, 4, and 6, that the circuitry is a dynamically adjustable crossbar switch (col. 9, lines 7+).

Regarding claim 14, Rangasayee discloses at least in Figs. 3, 4, and 6, a method of improving connectivity between signaling input/output (I/O) and an intellectual property block (102, 104) in a programmable logic resource (200) comprising:

driving a signal to a fixed pin location (inherently coupled to 170-173) upon which a package (IC; col. 1, lines 31+), having embedded therein the programmable logic resource (200), is mounted;

routing the signal from the fixed pin location to a nearest available I/O port (170-173) located along the periphery of the programmable logic resource; and

configuring a crossbar switch (250, 252, 280; col. 6, lines 58+) to route the signal from the nearest available I/O port to a corresponding data port (inherent for memory block 104) in the intellectual property block for processing.

Regarding claim 15, Rangasayee discloses at least in Figs. 3, 4, and 6, that driving the signal comprises sending the signal as output from one of processing circuitry and a memory (see col. 9, lines 7+).

Regarding claim 16, as for the recitation, "the signal is a low voltage differential signal", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claim 17, Rangasayee discloses at least in Figs. 3, 4, and 6, decoding the signal received from the nearest available I/O port (any one of 170-173) for output to the crossbar switch (250, 252, 280).

Regarding claim 18, Rangasayee discloses at least in Figs. 3, 4, and 6, configuring the crossbar switch during initial configuration of the programmable logic resource (see col. 6, lines 58+).

Regarding claim 19, Rangasayee discloses at least in Figs. 3, 4, and 6, configuring the crossbar switch during reconfiguration of all or part of the programmable logic resource (col. 7, lines 3+; col. 9, lines 7+).

Regarding claim 20, Rangasayee discloses at least in Figs. 3, 4, and 6, dynamically adjusting the crossbar switch while data is processing in the programmable logic resource (col. 9, lines 7+).

Response to Arguments

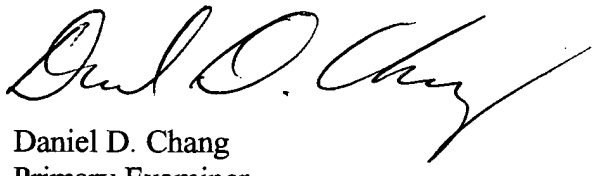
Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER